	US ATLAS PHASE II Upgrade BASIS of ESTIMATE (BoE)	Date of Est: November 16, 2015
		Prepared by: Verena I. Martinez Outschoorn, University of Illinois, Urbana-Champaign
		Docdb #: XXX

WBS number: X.X.X	WBS Title: MDT Hit Extractor Board and Firmware

WBS Dictionary Definition:

The Hit Extractor Board (HEB), located in the service cavern (USA15), contains the necessary hardware and firmware to receive the data from the MDT front end Chamber Service Module (CSM), provide buffering, data processing and event building, and interface with the trigger/DAQ systems. The work associated with this WBS is to design, fabricate and test the Hit Extractor Board, particularly the Mezzanine cards on the board. There is also work to develop the design in a test stand including an evaluation board.

The deliverables for this WBS are based on the ATCA proposal for ATLAS for Phase-II [1] and include 24 Hit Extraction Boards (comprised of 4 mezzanine cards, a carrier card and a rear transition module, RTM), 2 ATCA crates and additional modules to provide TTC and DCS. Note a 10% contingency is assumed in this estimate for the Hit Extraction Boards, for spares and may correspond to prototypes if successful.

Estimate Type (check all that apply – see BOE Report for estimate type by activity):

___ Work Complete
___ Existing Purchase Order
___ Catalog Listing or Industrial Construction Database
___ Documented Vendor Estimate based on Drawings/ Sketches/ Specifications
_X_ Engineering Estimate based on Similar Items or Procedures
___ Engineering Estimate based on Analysis
_X_ Expert Opinion

Supporting Documents (including but not limited to):

Details of the Base Estimate (Explanation of the Work)

This BOE covers the engineering, fabrication and testing costs of the Hit Extractor Boards for the MDT detectors, as well as the associated firmware development. The BOE also covers the engineering, fabrication and testing costs of preliminary prototype cards and a development test stand for the Hit Extractor system.

The set of deliverables are:
- Hardware to operate the Hit Extractor system. It is estimated to be achievable with 2 ATCA crates, 24 Hit Extraction Boards (comprised of 4 mezzanine cards, a carrier card and a rear transition module, RTM) and additional modules to provide TTC and DCS. Note a 10%

contingency is assumed in this estimate for the Hit Extraction Boards, for spares and may correspond to prototypes if successful.

- Assembly of mezzanine cards and possibly carrier and RTM modules.
- Firmware to operate the hardware with the desired functionalities.
- Integration and testing in the fully loaded crates.

The estimate is shown in Tab.1, including the labor cost including fringe and overhead for 1 FTE/year of a senior engineer and 1 FTE/year of an electronics technician, as well as the material and travel costs. More details regarding how these estimates are derived are provided in the next section. Estimates for FY19 are provided even though this is part of the pre-construction budget and is not included in the total.

WBS	Description	AY k$	FY19	FY20	FY21	FY22	FY23	Total (k$) FY20-FY23
6.6	**Muon**	**Total**						
6.6.4	**Muon_Illinois**	**Total**	322.94	337.17	346.69	348.49	358.58	**2157.85**
		Labor	307.94	317.17	326.69	336.49	346.58	1326.93
		Material	5.00	10.00	10.00	2.00	2.00	24.00
		Travel	10.00	10.00	10.00	10.00	10.00	40.00
		CORE					766.92	766.92
		FTEs	2.00	2.00	2.00	2.00	2.00	8.00
6.6.4.4	**HEB**	**Total**						2157.85
		Labor	307.94	317.17	326.69	336.49	346.58	1326.93
		Material	5.00	10.00	10.00	2.00	2.00	24.00
		Travel	10.00	10.00	10.00	10.00	10.00	40.00
		CORE					766.92	766.92
		FTEs	2.00	2.00	2.00	2.00	2.00	8.00
	Design	**Total**						337.17
		Labor	307.94	317.17				317.17
		Material	5.00	10.00				10.00
		Travel	10.00	10.00				10.00
		CORE						0.00
		FTEs	2.00	2.00				2.00
	Prototype	**Total**						346.69
		Labor			326.69			326.69
		Material			10.00			10.00
		Travel			10.00			10.00
		CORE						0.00
		FTEs			2.00			2.00
	Production	**Total**						1473.99
		Labor				336.49	346.58	683.07
		Material				2.00	2.00	4.00
		Travel				10.00	10.00	20.00
		CORE					766.92	766.92
		FTEs				2.00	2.00	4.00

Table 1: Cost estimate for the Hit Extractor system for the MDT detectors.

Justification of labor costs

The predicted personnel for the construction of the Phase II MDT Hit Extractor system are indicated in Tab. 2. The labor rates assumed are based on the manpower available at the University of Illinois, Urbana-Champaign, for the different types of labor (engineering or technician) and include fringe and overhead. The development is led by the Senior Engineers (Mike Kasten and Todd Moore), whose tasks include board design, firmware development, testing of fixtures, debugging and production. In addition, the efforts of an electronics-engineering assistant (Allison Sibert) are to assist in testing and debugging, as well as the assembly for production.

Description	FTEs & Hourly Rate	FY19		FY20		FY21		FY22		FY23	
		FTE	$/hr	FTE	$/hr	FTE	$/hr	FTE	$/hr	FTE	$/hr
Muon											
Muon_Illinois											
HEB											
Design											
	Sr EE	1.00	113.14	1.00	116.54						
	Elec. Tech.	1.00	60.25	1.00	62.05						
Prototype											
	Sr EE					1.00	120.03				
	Elec. Tech.					1.00	63.91				
Production											
	Sr EE							1.00	123.63	1.00	127.34
	Elec. Tech.							1.00	65.83	1.00	67.80

Table 2: FTEs requested and hourly rate for labor costs. Sr EE corresponds to a Senior Electronics Engineer and Elec. Tech. corresponds to an electronics technician.

Justification of material costs

In addition to personnel, some support is requested for materials and supplies, mainly for prototype mezzanine and carrier cards, and a transition module, as well as the additional modules from ATLAS, to be tested in the ATCA crate available at Illinois. These costs are estimated based on a test stand recently purchased at Illinois for another ATLAS project, as well as previous experience in similar projects at Illinois.

Justification of travel costs

Additional support is requested for travel to CERN for the engineer to attend meetings and workshops, to perform tests, and to collaborate with other members of the upgrade effort. The design, prototyping and construction of the Hit Extractor system is expected to require about 3 trips per year. In particular, the estimate includes 2 trips to CERN, which typically cost ~$3k (the total including overhead is therefore ~$7.5k) to attend a Muon or Upgrade Week at CERN and to participate in testbeam or integration tests at CERN. One additional domestic trip is also anticipated each year to work with the developers of the front-end electronics at Michigan, BNL, Arizona or Boston. The cost of this trip is typically in the $1-2k range, which with domestic overhead, totals about $2.5k. The total estimated cost is of ~$10k per year. The cost estimates are based on reviews of current airfares and past travel costs.

Justification of the Core estimate

A brief description of the functionalities of the Hit Extractor board is provided in the Comments section below. The estimated scale of the Hit Extractor system is based on:

- the number of input channels from the CSMs (~1100 input CSM to HEB links)[1]
- the data bandwidth requirements (~3.6 Gbps per input channel)[2]
- the memory needs to buffer the MDT data for L0 and L1 latencies of ~ 6μs and ~ 60μs respectively
- a preliminary estimate of the resources needed to perform the signal processing tasks, including tasks such as: event building when trigger signals are received, extraction of low resolution data to send to the MDT trigger, etc.
- providing interfaces to the DAQ, TTC and DCS.

The cost estimates for construction are derived from recently listed costs for an ATCA-based platform, comprised of:

- *ATCA shelf (partition):* houses the electronics boards, provides power and communication.
- *Mezzanine cards:* these mezzanines include the connections to the chambers, the output to the trigger, and the FPGAs that buffer and process the data.
- *ATCA carrier boards:* these boards house the mezzanine cards, handle signals from the TTC, the DCS and the network-based DAQ (FELIX).
- *Transition module:* these modules are connected to the shelf in the back of the slots and provide the communication with the TTC, the DCS and the DAQ. They also provide ethernet communication to perform functions such as configure the FPGAs remotely.
- *Additional modules:* These are for TTC, DCS, etc and would be included in each ATCA shelf.

The total estimated cost of the materials for production and assembly of a Hit Extractor system able to handle 1152 inputs is ~ $770 k. Figure 1 shows a schematic of the proposed hardware implementation. Table 3 shows a breakdown of the materials and fabrication costs estimated for the production of a full Hit Extractor system. The basic unit is an ATCA board and 24 boards are estimated to be able to handle the full readout of the MDTs and fit in two ATCA crates (for 14 slot crates). Note 2 slots in each crate are made available for modules to handle the TTC and DCS signals. Each ATCA board is comprised of 4 mezzanine cards, each at an estimated cost of about $4k, a carrier card of about $7k and an RTM of about $3k.

The costs provided here assume that all pieces of the system are designed and produced at Illinois. However, given the relatively modest requirements for the carrier card and the RTM, it is interesting to consider available options for carrier cards and RTMs already developed for other projects in ATLAS or even commercially available. In the case of the mezzanine cards, the project would benefit from a specific solution such as the one proposed to address the particular requirements of the Hit Extractor system. The proposal is a simple and cost-effective option that could provide a compact system to handle the significant number of input channels arriving from the MDT chambers.

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[1] An important consideration determining the scale of the system and ultimately the cost estimate is the number of input channels, corresponding to the number of CSM links. Accounting for the addition of a few new chambers (BME/BMR, BOE/BOR, BMG) and the subtraction of the chambers that are going to be replaced in the New Small Wheel Phase I upgrade (EI), the total number of expected input fibers is 1076.

[2] This rate is estimated derived from studies of expected rates based on measurements from data and simulation [2-4]
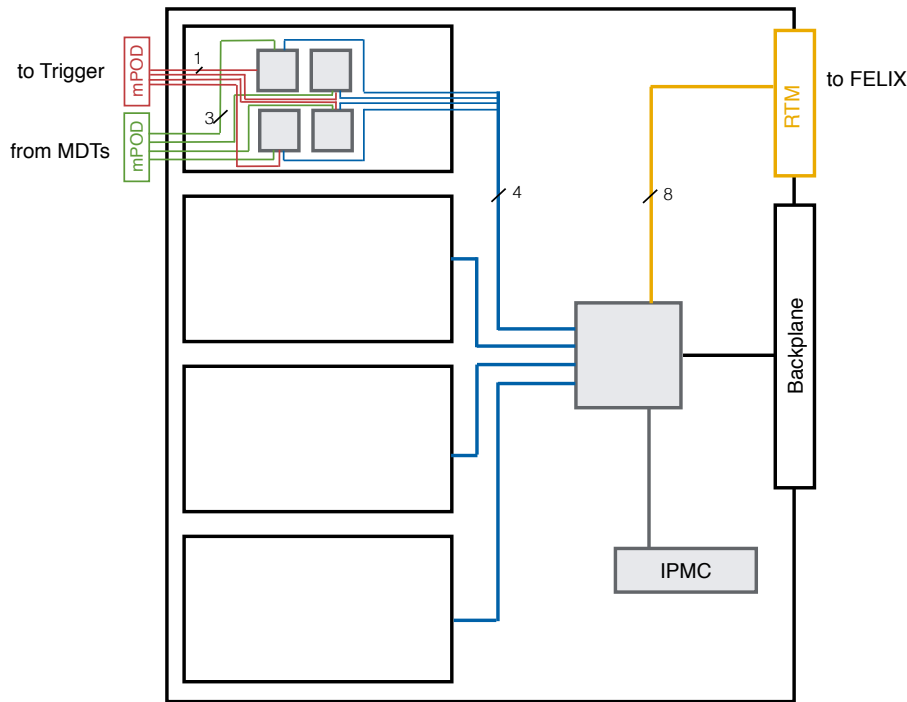
Figure 1. Schematic diagram of the implementation of the Hit Extractor Board in which four Advanced Mezzanine Cards (AMCs) are mounted on a carrier board. The various line colors represent different communication functionalities: inputs from MDTs (CSM), outputs to the muon trigger, outputs to the readout FELIX, etc.

The inputs are connected to the mezzanine cards and enter the FPGAs via MiniPOD 12 channel connectors. The output to the trigger could also be provided via the mezzanine card through a MiniPOD connector. These are compact connectors that provide an interested solution given the large number of input channels that we seek to accommodate in a small system to keep costs down. The signals from incoming and outgoing fibers need to be routed to the MiniPOD inputs. A possible solution is indicated in the table and the corresponding cost (called adaptors for MiniPOD connections).

The choice of FPGA needs to be further explored and validated. For this estimate, we determined the choice based on
- the number of transceivers to accomodate the inputs, outputs and other signals
- the amount of memory needed to buffer the data for the duration of the L0 and L1 latencies
- cost

Note that given the amount of memory necessary to buffer for the data for the duration of the L0 and L1 latencies, we propose to buffer all the data on RAM on the FPGA itself, instead of relying on external memory. This should be possible at a modest cost and greatly simplifies the design. Given these considerations, the Kintex-7 FPGAs from Xilinx are considered a viable option. Figure 3 (at the end of this document) shows the available options for this FPGA series. The XC7K160T has been identified as a possible candidate for FPGA that would satisfy the requirements of the project, while maintaining a low-cost ($340 per FPGA, with 4 FPGAs per mezzanine). One possibility considered is

to use a single FPGA per mezzanine for 12 input channels. However, the cost of an FPGA with sufficient transceivers and memory to perform the tasks more than doubles the cost. An open question is the requirement on the available resources on the FPGA. We plan to perform a detailed assessment of the resources needed to perform the functions required of the system (trigger matching, extraction of low resolution hits, etc) in the R&D phase of the project. Additional functionalities can be implemented in the carrier board, with a suggested Virtex-7 FPGA from Xilinx, as used in the LAr Phase-I upgrade of ATLAS (XC7VX550T-1FFG1927C).

Components	Count	Cost/Item ($)	Unit Cost ($)	Total (k$)
Hit Extractor Board (HEB)				**767**
ATCA System	2		**15000**	30
includes Chassis - Shelf, Shelf Manager, Power Supply				
Mezzanine Card	106		**3885**	412
Kintex 7 FPGA (8 GTX, XC7K160T-2FBG676)	4	340	1360	
miniPod Rx (12ch)	1	250	250	
miniPod Tx (12ch)	1	375	375	
other components	1	500	500	
PCB, assembly	1	1400	1400	
ATCA Blades	26		**6886**	179
Virtex 7 FPGA (80 GTX, XC7K160T-2FBG676)	1	4886	4886	
Front Panels	1	200	200	
Other components	1	500	500	
PCB, Assembly	1	1300	1300	
Transition Module	26		**3000**	78
miniPod Rx (L0/L1)	1	250	250	
QSFPs (FELIX)	3	250	750	
Rear Panels	1	200	200	
Other Components	1	500	500	
PCB, Assembly	1	1300	1300	
Adaptors for miniPod Connections	238		**202**	48
MTP-MTP Bulkhead adapter (12 ch)	1	22	22	
Cable with MTP, 6 inches (12 ch)	1	180	180	
Additional Modules	2		**10000**	20
for TTC, DCS for each partition				

Table 3: Cost estimate for the Hit Extractor system for the MDT detectors. This estimate is derived using an ATCA hardware platform. The components are estimated using current costs and are quoted in USD. Note 10% of spares are included for the mezzanine cards, carrier cards and RTMs.

Given the maximum expected hit rates, the input channels are expected to carry maximum rates of ~3.6 Gbps. Given these rates, each ATCA blade can include 4 MiniPOD connections for the input, corresponding to 48 channels per board. This implies that all the fibers can be read out by ~23 boards, but we propose to segment the system into 24 in order to group links that are logically connected. Additional boards are used for the TTC and DCS signals. Since the ATCA crates house up to 14 boards and 2 slots in each are for TTC and DCS, 2 crates provide 24 slots and hence are sufficient for the

whole system. Table 2 shows a breakdown of the construction costs estimated for the Phase II MDT Hit Extractor system. The choice of a MiniPOD allows us to increase the increase the number of input and output channels per board, due to the smaller connector size, compared to alternatives such as QSFPs. This also allows us to minimize the size of the system, also considering the cost.

The costs for parts are determined from parts distributors such as allied, avnet or digikey. As an example, the quote for the FPGA for the mezzanine card is included in Fig. 4 at the end of this document and the quote for the FPGA for the carrier card is included in Fig. 5. The PCB and assembly costs are estimated from previous designs. The assembly costs in particular are based on contract assembly estimates. One option to be explores is to increase the assembly effort at Illinois from Allison, the engineering-technician, that may reduce the PCB assembly costs and hence the overall cost of the project. This would depend on time, since the work performed in house is expected to be slower than in industry. Other items, such as the ATCA crates are determined from other ATLAS subsystems that have purchased them for their own upgrades.

Assumptions:

Several assumptions have been made to make this cost estimate.
- The ATCA hardware platform that is a standard for ATLAS upgrades has been selected to determine the costs of construction (based on a 14-slot crate)
- The approximate number of transceiver channels is ~ 1100
- The same number of output channels to the trigger is made available in order to minizimize the latency.
- The estimated maximum data bandwidth necessary is ~3.6 Gbps per chamber (200 Mbps per front-end Mezzanine card)

Risk Analysis:

Schedule Risk: Probability: low, impact: low, overall score: low.
      Potential problems: The main concern for the schedule at the moment is the support and availability for technically experienced manpower (engineers and technicians).
      Mitigation: Provide support for the engineers and technician to support R&D activities as soon as possible.

Cost Risk: Probability: medium, impact: low, overall score: low.
      Potential problems: The cost is driven by the size of the system to be built, the choice of FPGAs and the assembly costs.
      Mitigation: Perform R&D studies to provide a detailed system design.

Technical/Scope Risk: Probability: medium, impact: low, overall score: low
      Potential problems: The size of the system may change substantially depending on the number of channels needed or if the processing needs are higher than expected and a more powerful FPGA is necessary. Another issue that can significantly increase the complexity of the readout is the possibility of reading out legacy electronics due to the difficult access to some of the chambers in the muon barrel.
      Mitigation: Begin R&D studies of the performance of the proposed design and possible alternatives as soon as possible.

Contingency Rules Applied:

to be assigned by L2 managers and project office

Dependence of your deliverable on "external"factors:

At the moment we do not foresee a strong external dependence. If the carrier card and RTM are purchased from another group, we will depend on their availability. Integration and commissioning will depend strongly on the available of front-end hardware and how advanced the trigger and DAQ systems are.

Comments & Supporting Documentation:

Brief description of the functionality of the proposed system

This is a proposal to fund the development and production of a board for the Phase II upgrade of the Monitored Drift Tube (MDT) read-out system in ATLAS at the University of Illinois, Urbana-Champaign. The Hit Extractor Board (HEB) would be located in the service cavern (USA15) and its main functions are to receive the data from the MDT front end, provide buffering, data processing and event building, and interface with the trigger/DAQ systems.

We propose to develop a design of a digital electronics board that could be built by US ATLAS, the Hit Extractor Board. This board would operate in the ATLAS service cavern for Phase II.
The Hit Extractor Board aims to:

- receive the data from the front-end boards
- provide data buffering
- provide data processing for event building and trigger
- deliver low-latency, low-granularity signals to the hardware trigger
- interface with the network-based trigger/DAQ system
- provide configuration and monitoring capabilities.

As shown in Fig. 2, the proposed Hit Extractor Board includes a polling loop that examines the incoming data input from high-speed fibers. Each fiber serves an MDT chamber and is connected to the CSM board which in turn multiplexes up to 18 front end mezzanine cards that each multiplex signals from 24 channels (MDT tubes). The total data bandwidth expected is at most 200Mbps from each mezzanine, resulting in about 3.6 Gbps per CMS to HEB link. These links are expected to be implemented in using the CERN GBT link [5] that can achieve 4.8 or 9.6 Gbps.

The available data is stored in a pipeline memory until a Level-0 signal is received. Buffered hits are matched to the trigger by extracting the data acquired in a time window specified by the Level-0 trigger time. The time window is defined by the offset corresponding to the beginning of a trigger time, the size of the window to accommodate the maximum drift time and the option of looking for hits in a preceding or following time window. Hits satisfying the Level-0 trigger are passed along to a second pipeline memory until a Level-1 signal is received. Hits are then associated to the trigger time and the data satisfying the Level-1 trigger is sent to the network-based DAQ system, FELIX.
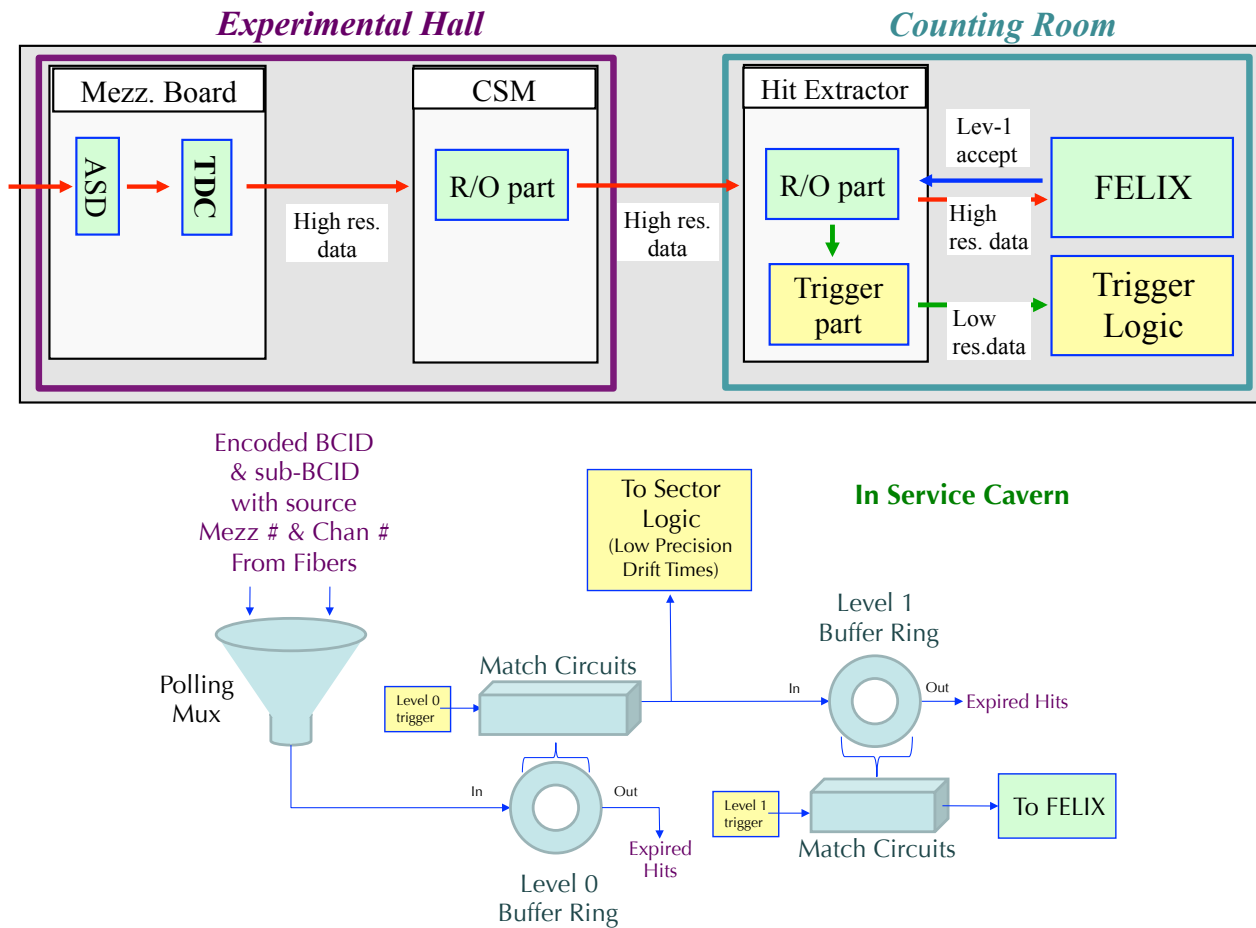
Figure 2. Schematic of the Hit Extractor Board (HEB) in a MDT read-out scheme where all data is sent to the service cavern without a trigger signal and is stored in pipeline memories there.

UIUC Electronics Effort for Proposed Activities

A team at UIUC is available to participate in the Phase-II upgrade of the Muon electronics, led by Verena I. Martinez Outschoorn, together with research staff and physicists. UIUC has expertise in digital electronics for trigger/DAQ and on MDT detectors. Two electrical engineers (Mike Kasten and Todd Moore) and an electronics-engineering assistant (Allison Sibert) have experience in trigger and DAQ electronics for several experiments including ATLAS. The group has the technical expertise and infrastructure to develop digital electronics including design, production, testing, and firmware and software development. Kasten has experience in trigger electronics in CDF and has designed the SSB board for the ATLAS FastTracKer (FTK). Moore's previous experience includes the design, assembly and testing of data acquisition boards for the CDF muon readout system and the Mu2e calorimeter, and electronics for the Dark Energy Survey. In addition, Verena Martinez Outschoorn has five years of dedicated experience on MDTs. The project is therefore a match to the skills and expertise in the group.

References

[1] S. Ballestrero et al., *ATCA in ATLAS*, EDMS ATU-GE-ES-0001 (2014), https://edms. cern.ch/edmsui/file/1304001/1/ATCA-Backupdoc-rev2.pdf.

[2] G. Aielli et al. *Cavern background measurements and comparison with simulation*, ATL-COM-MUON-2013-003, CERN, Geneva (2013), https://cds.cern.ch/ record/1513176.

[3] S. Sun et al., Predicting Hit Rates in the ATLAS Monitor Drift Tube at 10^{34} cm^{-2}s^{-1} at $\sqrt{s}$ = 7 and 8 TeV, ATLAS Muon Communication ATL-COM-MUON-2013-011 (2013), https://cds.cern.ch/record/1548125.

[4] Y. Chan et al., *Expected Muon Spectrometer Background in Run 2*, ATL-MUON-INT-2014-004 (2014), https://cds.cern.ch/record/1707800.

[5] P.Moreira et al., *The GBT-SerDes ASIC prototype*, Journal of Instrumentation 5 11 (2010) C11022, URL http://stacks.iop.org/1748-0221/ 5/i=11/a=C11022.

Kintex®-7 FPGAs

Kintex®-7 FPGAs
Optimized for Best Price-Performance
(1.0V, 0.95V, 0.9V)

	Part Number	XC7K70T	XC7K160T	XC7K325T	XC7K355T	XC7K410T	XC7K420T	XC7K480T
	EasyPath™ Cost Reduction Solutions[1]	–	–	XCE7K325T	XCE7K355T	XCE7K410T	XCE7K420T	XCE7K480T
Logic Resources	Slices	10,250	25,350	50,950	55,650	63,550	65,150	74,650
	Logic Cells	65,600	162,240	326,080	356,160	406,720	416,960	477,760
	CLB Flip-Flops	82,000	202,800	407,600	445,200	508,400	521,200	597,200
Memory Resources	Maximum Distributed RAM (Kb)	838	2,188	4,000	5,088	5,663	5,938	6,788
	Block RAM/FIFO w/ ECC (36 Kb each)	135	325	445	715	795	835	955
	Total Block RAM (Kb)	4,860	11,700	16,020	25,740	28,620	30,060	34,380
Clock Resources	CMTs (1 MMCM + 1 PLL)	6	8	10	6	10	8	8
I/O Resources	Maximum Single-Ended I/O	300	400	500	300	500	400	400
	Maximum Differential I/O Pairs	144	192	240	144	240	192	192
	DSP48 Slices	240	600	840	1,440	1,540	1,680	1,920
Integrated IP Resources	PCIe® Gen2[2]	1	1	1	1	1	1	1
	Analog Mixed Signal (AMS) / XADC	1	1	1	1	1	1	1
	Configuration AES / HMAC Blocks	1	1	1	1	1	1	1
	GTX Transceivers (12.5 Gb/s Max Rate)	8	8	16	24	16	32	32
Speed Grades	Commercial	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2
	Extended	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3
	Industrial	-1, -2	-1, -2, -2L	-1, -2, -2L	-1, -2, -2L	-1, -2, -2L	-1, -2, -2L	-1, -2, -2L

Available User I/O: 3.3V HR I/O, 1.8V HP I/O, 1.8V HP I/Os (GTX)

Package[3]	Dimensions (mm)	XC7K70T	XC7K160T	XC7K325T	XC7K355T	XC7K410T	XC7K420T	XC7K480T
FBG484 / FBV484	23 x 23	185, 100 (4)	185, 100 (4)					
FBG676 / FBV676	27 x 27	200, 100 (8)	250, 150 (8)	250, 150 (8)				
FFG676 / FFV676	27 x 27		250, 150 (8)	250, 150 (8)		250, 150 (8)		
FBG900 / FBV900	31 x 31			350, 150 (16)		350, 150 (16)		
FFG900 / FFV900	31 x 31			350, 150 (16)	300, 0 (24)	350, 150 (16)		
FFG901 / FFV901	31 x 31						380, 0 (28)	380, 0 (28)
FFG1156 / FFV1156	35 x 35						400, 0 (32)	400, 0 (32)

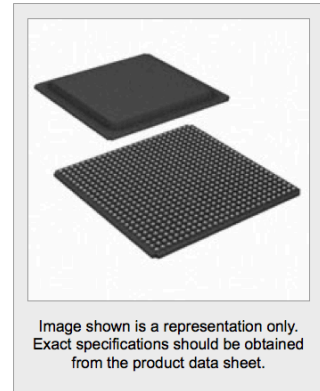**FBG / FBV:** 1.0 mm Lidless flip-chip; **FFG / FFV:** 1.0 mm Flip-chip fine-pitch

Notes: 1. EasyPath™ solutions provide a fast and conversion-free path for cost reduction.
2. Hard block supports PCI Express Base 2.1 specification at Gen1 and Gen2 data rates. Gen3 supported with soft IP.
3. See DS180, *7 Series FPGAs Overview* for package details.

XMPO85 (v3.8)

Figure 3: Table summarizing the Kintex-7 products from Xilinx.

		All prices are in US dollars.		
Digi-Key Part Number	XC7K160T-2FBG676I-ND	**Price Break**	**Unit Price**	**Extended Price**
Quantity Available	0 Enter Quantity Requested	1	345.00000	345.00
Manufacturer	Xilinx Inc.			
Manufacturer Part Number	XC7K160T-2FBG676I			
Description	IC FPGA 250 I/O 676FCBGA			
Lead Free Status / RoHS Status	Lead free / RoHS Compliant			
Moisture Sensitivity Level (MSL)	4 (72 Hours)			

Quantity	Item Number ?	Customer Reference	
1	XC7K160T-2FBG676I-ND		Add to Cart

Image shown is a representation only. Exact specifications should be obtained from the product data sheet.

When requested quantity exceeds displayed pricing table quantities, a lesser unit price may appear on your order. You may submit a request for quotation on quantities which are greater than those displayed in the pricing table.

Datasheets	7 Series FPGAs Overview
	Kintex-7 FPGAs Datasheet
	Kintex-7 FPGAs Brief
Product Photos	676-FCBGA
Product Training Modules	Powering Series 7 Xilinx FPGAs with TI Power Management Solutions
PCN Design/Specification	Zynq-7000 Datasheet Update 02/Jun/2014
PCN Assembly/Origin	Additional Wafer Fabrication 16/Dec/2013
	Substrate Supplier Addition 03/Nov/2014
Standard Package ?	1
Category	Integrated Circuits (ICs)
Family	Embedded - FPGAs (Field Programmable Gate Array)
Series	Kintex-7
Number of LABs/CLBs	12675
Number of Logic Elements/Cells	162240
Total RAM Bits	11980800
Number of I/O	250
Number of Gates	-
Voltage - Supply	0.97 V ~ 1.03 V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C
Package / Case	676-BBGA, FCBGA
Supplier Device Package	676-FCBGA (27x27)

Figure 4: Quote for Kintex-7 FPGA XC7K160T-2FBG676 from digikey. Screenshot captured 11/23/2015 from website: http://www.digikey.com/product-detail/en/XC7K160T-2FBG676I/XC7K160T-2FBG676I-ND/3911282

			All prices are in euro.	
Digi-Key Part Number	XC7VX550T-1FFG1927C-ND	**Price Break**	**Unit Price**	**Extended Price**
Quantity Available	0 Enter Quantity Requested	1	4.885,89000	4.885,89
Manufacturer	Xilinx Inc.			
Manufacturer Part Number	XC7VX550T-1FFG1927C			
Description	IC FPGA 600 I/O 1927BGA			
Lead Free Status / RoHS Status	Lead free / RoHS Compliant			
Moisture Sensitivity Level (MSL)	4 (72 Hours)			

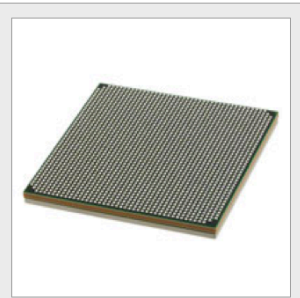| Quantity	Item Number ?	Customer Reference	
1	XC7VX550T-1FFG1927C-ND ⬍		Add to Cart

Image shown is a representation only. Exact specifications should be obtained from the product data sheet.

When requested quantity exceeds displayed pricing table quantities, a lesser unit price may appear on your order. You may submit a request for quotation on quantities which are greater than those displayed in the pricing table.

Datasheets	7 Series FPGAs Overview Virtex-7 T/XT FPGA Datasheet
Product Photos	XC7V2000T-1FLG1925CES9937
Product Training Modules	Powering Series 7 Xilinx FPGAs with TI Power Management Solutions
PCN Design/Specification	Zynq-7000 Datasheet Update 02/Jun/2014
PCN Assembly/Origin	Additional Wafer Fabrication 16/Dec/2013 Substrate Supplier Addition 03/Nov/2014
Standard Package ?	1
Category	Integrated Circuits (ICs)
Family	Embedded - FPGAs (Field Programmable Gate Array)
Series	Virtex®-7
Number of LABs/CLBs	43300
Number of Logic Elements/Cells	554240
Total RAM Bits	43499520
Number of I/O	600
Number of Gates	-
Voltage - Supply	0.97 V ~ 1.03 V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C
Package / Case	1924-BBGA, FCBGA
Supplier Device Package	1927-FCBGA (45x45)
For Use With	410-301P-KIT-ND - BOARD NETFPGA-SUME

Figure 5: Quote for Virtex-7 FPGA XC7VX550T-1FFG1927C from digikey. Screenshot captured 11/23/2015 from website: http://www.digikey.ch/product-detail/en/XC7VX550T-1FFG1927C/XC7VX550T-1FFG1927C-ND/3981998